Drawing Amendments

Applicant has submitted replacement sheets for FIGS. 1 and 2 to change the label of element 118 from "volatile memory" to "non-volatile memory" in accordance with the specification.

Remarks

The Official Action rejected claims 1-23. Applicant has amended FIGS. 1 and 2. Claims 1-23 as originally filed remain pending.

Claim Rejections - 35 USC § 102

The Official Action rejected claims 1-23 under 35 USC 102(b) as being anticipated by William et al (US 6,199,151). Applicant respectfully requests the rejection of claims 1-23 be withdrawn in light of the following.

Claims 1-7

Claims 1-7 require a configuration store to select between an encoded chip select mode and an unencoded chip select mode. The Official Action appears to rely on column 6 lines 12-26 of William for an inherent teaching of a register to indicate using either encoded or unencoded chip selects. In this section, William teaches "an alternate embodiment" in which unencoded row values may be stored in the TLB 25 instead of encoded row values as previously described. Moreover, William teaches "yet another embodiment" in which partially encoded row values may be stored in the TLB 25. Thus, William appears to teach three embodiments: a first embodiment that uses encoded row values, a second embodiment that uses unencoded row values, and a third embodiment that uses partially encoded row values. However, Applicant has been unable to locate any teaching in William of an embodiment in which the type of row value (e.g. encoded, unencoded, partially encoded) may be programmatically selected as suggested by the Official Action. Instead, William appears to teach an apparatus that uses only one of the three identified types of row values. Since William does not appear to explicitly or inherently teach an apparatus

that may select between an encoded chip select mode and an unencoded chip select mode, William fails to anticipate the invention of claims 1-7.

Claim 7

Claim 7 further requires an address decoder to generate the encoded chip select word ***such that a lowest order bit of the encoded chip select word is the only active bit*** of the encoded chip select word, and to generate the unencoded chip select word ***such that a lowest order bit of the unencoded chip select word is the only active bit*** of the unencoded chip select word. William appears to provide no teaching regarding the above encoding scheme. The Official Action even appears to indicate that William provides no such teaching since the Official Action states William would need to be modified in order to meet the limitations of claim 7 as evidenced by the statement "Although in William's Fig. 3 the encoded value start from 0, 1, to 7[, i]t would have been an obvious modification that the encoded row value to start from 1, 2 ... 7 to 0." The Official Action further supports its 102 rejection of claim 7 by pointing out that William has anticipated some variation in the encoding implementation.

However, despite William disclosing an encoding scheme in Fig. 3 and indicating that some other encoding scheme may be used without departing from the spirit and the scope of the invention of William, William simply does not disclose inherently or explicitly the encoding scheme claimed by claim 7 and therefore does not anticipate the invention of claim 7. Applicant respectfully points out that claim 7 was rejected under 102 and not under 103. As a result, whether "it would have been an obvious modification that the encoded row value to start from 1, 2 ... 7 to 0" has

no bearing on an anticipation rejection. Applicant respectfully requests that the anticipation rejection of claim 7 be withdrawn.

In order to expedite prosecution, Applicant points out that it would not be obvious to modify William in the proposed manner. In support of this proposition, the following provides technical information that is not necessarily reflected in the language of claim 7. Such information is not being used to distinguish claim 7 from William but is being used to indicate why the distinguishing limitations of claim 7 are not obvious in light of William.

William appears to briefly indicate that the encoding scheme of the row values may be modified. However, William appears to provide no motivation to modify the encoding scheme in a manner so as to arrive at the Applicant's invention of claim 7. In the William system, one encoding scheme is just as good as another and the one disclosed by William appears to be the most natural for encoding TLB row values. While William appears to address issues involving row values stored in a TLB 25, William appears to provide only minor teaches regarding the boot or startup process. For example, see William at column 5, lines 42-48 regarding a brief description of initialization code of a BIOS device. In light of this brief teaching, the Official Action attempts to provide further details by assuming that William uses an Intel Architecture (IA) environment wherein the boot code is assigned from 0 to 1 Mbyte. However, in such an IA environment, the processor initially only uses physical addressing (sometimes referred to as real mode addressing) to address and execute initialization code from the boot nub since virtual addressing hardware such as the TLB 25 of William is not configured until the operating system is executed. One of the early stages of operating system execution is to configure the TLB and virtual

addressing hardware so the processor may switch from real mode to protected mode.

The encoding scheme of claim 7 is useful for boot code because the scheme ensures that the same chip select bit (e.g. lowest order bit) is active regardless of the present configuration of the system such as whether address decoder is in an encoded chip select mode or an unencoded chip select mode. Accordingly, the chip select mode may be changed from one mode to another mode while executing the boot nub without changing which memory device is selected, thus ensuring the memory device with the boot nub remains selected. Accordingly, since William appears to be addressing how to store row values in a TLB 25 and not issues regarding the boot sequence, William appears to provide no teaching or suggestion to modify the encoding scheme of the row values to arrive at the invention of claim 7.

Claims 8-12

Claims 8-12 require a plurality of memory devices comprising a memory device with a boot code nub and an apparatus to generate an encoded or unencoded chip select word that selects the memory device with the boot code nub. While William may disclose a plurality of memory devices 16A-C, 17A-C, 18A-C selected by chip selects CS1, CS2, etc., William appears to indicate that the initialization code is in a BIOS device separate from the memory devices 16A-C, 17A-C, 18A-C. See, column 5, lines 42-48 of William. William appears to provide very few details regarding the BIOS device and in particular appears to provide no teaching regarding using encoded or unencoded chip selects to address the BIOS device. Accordingly, William does not appear to teach generating encoded or

unencoded chip select words ***to select a memory device with the boot code nub*** as required by claims 8-12.

Claims 13-23

Each of claims 13-23 require generating an unencoded chip select word that comprises an encoded chip select word of a boot code nub in response to an address for the boot code nub and an unencoded chip select mode. As stated above, William appears to provide no teaching regarding generating chip selects for the BIOS device. Moreover, as stated above, William may disclose an encoding scheme in FIG. 3 for rows of a TLB 25, but there is no indication which line, if any, of FIG. 3 corresponds to the BIOS device. Therefore, William does not appear to teach the claimed relationship between the unencoded chip select word and the encoded chip select word for the boot code nub in which the unencoded chip select word comprises the encoded chip select word. Accordingly, William does not anticipate claims 13-23.

Conclusion

The foregoing is submitted as a full and complete response to the Official Action. Applicant submits that all remaining claims are in condition for allowance. Reconsideration is requested, and allowance of all remaining claims is earnestly solicited.

Should it be determined that an additional fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #02-2666. If the Examiner believes that there are any informalities which can be corrected by an Examiner's amendment, a telephone call to the undersigned at (503) 439-8778 is respectfully solicited.

Respectfully submitted,

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